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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,188	03/11/2004	Taiji Ema	960045E	4959

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EXAMINER	
UMEZ ERONINI, LYNETTE T	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,188	EMA ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-18* is/are rejected.

7)☒ Claim(s) *2 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/11/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/05 & 1/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 4/9/05 and 1/3/06 has considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 3, 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minami (US 4,252,840) in view of Dennison et al. (US 5,338,700).

As to claims 1, 3, 4 and 15, Minami discloses patterning a gate oxide layer **3** and a polycrystalline silicon gate electrode **4** on a silicon substrate **1** (column 2, lines 3-15 and FIG. 1A); forming a first (oxide) insulating layer **7** on the substrate, forming a second (phosphorus glass) insulating layer **10** on the first oxide insulator **7**, and depositing a third (Si_3N_4) layer **11** on insulating layer **10** (column 2, lines 21-40); etching the second and third insulating layers, **10, 11** by patterning a mask for boring an electrode contact hole, where the second and third insulating layers **10** and **11** are etched by different etchants (column 2 line 61- column 3, line 2); and etching the first insulating **7** thereby providing contact hole **12** (column 3, lines 2-19). Minami also teaches the first, second and third insulating layers **7, 10, and 11** are etched at different rates (column 2, line 55 - column 3, line 10 and 20-22). The above reads on,

A method for fabricating a semiconductor device comprising the steps of:

forming a conductor pattern over a semiconductor substrate;

forming a first insulation film covering the conductor pattern;

forming over the first insulation film a second insulation film having etching characteristics different from those of the first insulation film;

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film;

forming over the third insulation film a mask layer; and

forming a hole in the third insulation film, the second insulation film and the first insulation film;

the step of forming the hole including a first step of etching the third insulation, a second step of etching the second insulation film, and a third step of etching the first insulation film; an etching condition at the first step being different form that at the second step, **in claim 1**.

Minami differs in failing to disclose forming a first insulation film having a substantially flat surface, **in claim 1**.

Dennison discloses providing planarized insulating material (column 2, lines 52-55 and 61-63)"a planarized layer **28** such as BPSG . . . a thin layer **20** of Si_3N_4 (which is the same as applicants' first insulation layer) is provide atop the wafer . . ." (column 3, lines 34-36) and ". . . planarized first layer **28** (which is the same as applicants' first and second insulation layer) of an insulating material . . . which is planarized back by chemical mechanical polishing (CMP)" (column 3, lines 50-54). It is noted that there are no intrinsic properties obtained by planarizing a first and second insulation layer. An insulation layer can be planarized by chemical mechanical polishing not by virtue that it is a first or a second insulating film.

Since Dennison illustrates forming a planarized insulation film by chemical mechanical polishing is known, then it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Minami by planarizing an insulation layer as taught in the Dennison reference because planarizing an insulation layer is known to be effective in fabricating semiconductor devices.

Minami differs in failing to specify the etching rate of the second insulation layer and third insulation layer in forming the hole, as recited, **in claim 15**.

Minami illustrates that a hole is formed through different insulation layers using different etchant, thereby resulting in each insulation layer having a different etch rate. Hence it would have been obvious to one having ordinary skill in the art at the time the invention was made to select an etch rate of the second insulation layer as taught in the Minami reference, including Applicants' specifically claimed etching rate of the second insulation layer, which differs from the etch rate of the third insulation in the first step and differs from the second insulation in the second step, for the purpose of manufacturing a semiconductor device with good yield (column 1, lines 33-35).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 6-7; 9-10; and 12-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Ema et al. (US 6,744,091 B1).

As to claims 6-8; 9-11; and 12-14, Ema discloses a method for fabricating a semiconductor device with a self-aligned opening by patterning a conductor over a

semiconductor substrate; forming a first insulation film formed over the first conductor pattern; a second insulation film over the first insulation film, wherein the second insulation film having a substantially flat surface and having etching characteristics different from those of the first insulation film; a third insulation film formed over the second insulation film, the third insulation film having etching characteristics different from those of the second insulation film; and a fourth insulation film formed over the third insulation film, the fourth insulation film having etching characteristics different from those of the third insulation film; and forming an opening formed in the fourth insulation film, the third insulation film, the second insulation film, and the first insulation film, the opening being self-aligned with the first conductor pattern (Abstract). Ema further discloses source and drain layers **24** and **25** in silicon substrate **10** (**FIGS. 1** and **2**).

7. Claims 6, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ema (US '091 B1) as applied to claims 6-7; 9-10; and 12-13 respectively above.

Ema differs in failing to specify the etching rate of the third insulation layer in forming the hole, as recited, **in claims 16-18**.

Ema illustrates that a hole is formed through different insulation layers having different etching characteristics is known, thereby resulting in each insulation layer having a different etch rate. Hence it would have been obvious to one having ordinary skill in the art at the time the invention was made to select an etch rate of the third insulation layer as taught in the Ema reference, including Applicants' specifically claimed etching rate of the third insulation layer at the first step, which differs from the

etching rate of the fourth insulation in the first step and differs from the third insulation in the second step, for the purpose of manufacturing a semiconductor device, which can facilitate etching contact hole for a capacitor storage electrode can decrease the number of fabrication steps (Ema, column 3, line 66 – column 4, line 8).

Allowable Subject Matter

8. Claims 2 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: As to claims 2 and 5, the prior art of record taken alone or in combination fails to suggest, teach or render obvious in a method for fabricating the semiconductor device, further comprising; the step of forming the first insulation film, over the fourth insulation film so as to cover the conductor pattern, combination with the rest of the limitations of the claim.

Response to Arguments

10. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection because the former prior art of record failed to teach "the step of forming the hole including a first step of etching the third insulation film, a second step of etching the second insulation film and a third step of

etching the first insulating film, an etching condition at the first step being different from that at the second step" as recited in (Currently Amended) Claims 6, 9, and 12.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Art Unit 1765

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July 6, 2006

NADINE NORTON
SUPERVISORY PATENT EXAMINER